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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
WONG, LINDA	
ART UNIT	**PAPER NUMBER**
2634	

DATE MAILED: 12/10/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/955,693	CAO, JUN	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to because

   a. In Fig. 1, label for resister between Amp 130 and DC Correct 150 is necessary.

   b. In Fig. 4A, the labels 407 and 417 are used twice to describe two different aspects of the diagram.

   c. In Fig. 5, the labels 507 and 517 are used twice to describe two different aspects of the diagram.

   d. In Fig. 6, the label 676 is used twice to describe two different aspects of the diagram.

   e. In Fig. 5, the arrows indicating the current direction of the transistors, M5, M6 and M7, are not included in the diagram.

   f. In Fig. 13, the label 1315 is used twice to describe two different aspects of the diagram.

   Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities:

   a. In Fig. 2, the description of label 215 is not included in the specification.

   b. In Fig. 6, M7 675 and M8 680 are not described in the specification.

   c. On page 14, paragraph 58, line 7, the label 676 is used twice to describe two different aspects of the diagram, which causes confusion of which aspect of the diagram is input AP.

   d. The specification is missing a Field of Invention description.

   Appropriate correction is required.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 4, 7, 8, 9, 10, 11, 13, 16-18 are rejected under 35 U.S.C. 102(b) as being unpatentable by Hogge Jr. (US Patent No: 4535459)

   a. Regarding **claim 1,** line1, Hogge Jr. discloses a receiving clock signal (Fig. 4, label 124) and data signal (Fig. 4, label 100), a first signal (Fig. 4, label 112), a second signal (Fig. 4, label 122), a third signal (Fig. 4, input to 106 from 105) generated by delaying the data signal, an error signal generated by combining the first and third and a reference signal generated by combining the first and second signal.

c. Regarding **claim 4,** line 1, Hogge Jr. discloses two XOR gates that are used to provide an error and reference signal (Fig. 4, label 106 and 114).

d. Regarding **claim 7,** line 1, Hogge Jr. discloses a first storage device (Fig. 4, label 102) that receives and stores the data signal (Fig. 4, label 100) to generate the first signal (Fig. 4, label 112), a second storage device (Fig. 4, label 116) that receives and stores the first signal (Fig. 4, label 112) to generate a second signal (Fig. 4, label 122), a delay block (Fig. 4, labels 104 and 105 and 108 and 110) that receives and delays the data signal to produce a third signal (Fig. 4, input to 106 from 105), a logic circuit (Fig. 4, label 106) configured to combine the first and second signal and a logic circuit (Fig. 4, label 114) that can combine the first and third signal (Fig. 4, label 112 and input to 106 from 105).

e. **Claim 8** inherits all the limitations of claim 3.

f. Regarding **claim 9,** line 1, Hogge Jr. discloses a flip-flop and a latch receiving a clock signal. It is inherent in the prior art that a clock signal would comprise of edges, first and second levels. (Fig. 4, label 102 and 116)

g. Regarding **claim 10**, line 1, Hogge discloses a flip-flop that stores the data on the first edge and the latch latches on the second level (Fig. 5a, labels 100, 124, 105, 126).

h. Regarding **claim 11**, line 1, Hogge discloses a first edge that is falling and a second edge that is rising (Fig. 5a, label 126).

i. Regarding **claim 13**, line 1, Hogge discloses a flip-flop (Fig. 4, label 102) receiving a data input port (Fig. 4, label 100) and a clock input (Fig. 3, label 82 and 84) coupled to a clock port (Fig. 3, label 78), a latch (Fig. 3, label 50) having a data input coupled to an output of the first flip-flop (Fig. 3, label 48) and a clock input coupled to the clock port (Fig. 3, label 82), a delay element having an input coupled to the data input port (Fig. 4, labels 100, 104, 108, 105, 110), a first logic circuit (Fig. 4, label 106) having a first input coupled to the output of the flip-flop (Fig. 4, label 112) and a second input coupled to the output of the latch (Fig. 4, label 112) and a second logic circuit (Fig. 4, label 114) having a first input coupled to the output of the first flip-flop (Fig. 4, label 112) and a second input coupled to the output of the delay element. (Fig. 4, label 112)

j. **Claims 16 -18** inherits all the limitations of claim 4.

Claim Rejections - 35 USC § 103

4. **Claims 2, 5, 12, 14, 15, and 19-21** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge Jr. (US Patent No: 4535459) in view of Savoj (US Application No: 09/782687).

a. Regarding **claim 2**, line 1, Although Hogge failed to teach a loop filter receiving a reference and error signal, Savoj teaches a loop filter (Fig. 2, labels 220and 230) receiving an error and reference signal. It would be obvious to one skilled

in the art to pass an error and reference signal to a loop filter to accurately provide the control signal to the VCO.

b. Regarding **claim 5**, line 1, Although Hogge failed to teach the delay of the data signal is approximately equal to the clock-to-Q of the flip-flop, Savoj teaches such a limitation. Savoj discloses a third signal delayed by a flip-flop, which is approximately equal to the delay of the flip-flop that is used to generate the first signal. (page 4, paragraph [0045]) It would be obvious to one skilled in the art to improve performance by decreasing the delay time.

c. **Claim 12** inherits all the limitations in claim 5.

d. Regarding **claims 14 and 15**, line 1, Although Hogge fails to teach a first data input port is configured to receive a differential signal, Savoj teaches such a limitation. Savoj discloses that all the signal paths are differential. (page 4, paragraph [0042], lines 6-7 and lines 13-15) It would be obvious to one skilled in the art to reduce jitter caused by noise by using differential signals.

e. Regarding **claims 19 and 20,** line 1, Although Hogge fails to teach an optical receiver comprised of a phase detector, Savoj teaches such a limitation. Savoj discloses an optical receiver comprising of a phase detector, wherein the optical receiver comprises of an optical transmitter and an optical receiver coupled to the optical transmitter. (Fig. 1) It would be obvious to one skilled in the art to provide a system that can operate at high frequencies. (page 1, paragraph [0005] and [0006])

f. Regarding **claim 21,** line 1, Although Hogge fails to teach a system for receiving and transmitting optical signals, Savoj teaches such a limitation. Savoj discloses a receiving and transmitting optical signals comprising of a light emitting diode, a transmitter coupled to the light emitting diode, a photo-diode receiving optical signal, a receiving amplifier coupled to the photo-diode, and a phase detector coupled to the receive amplifier. (Fig. 1) It would be obvious to one skilled in the art to use this system that can operate at high frequencies. (page 1, paragraph [0005] and [0006])

5. **Claims 6, and 22-23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Hogge Jr. (US Patent No: 4535459) in view of Zhang (US Patent No: 6614371).

a. Regarding **claim 6**, line 1, Although Hogge fails to teach a circuit where the loads to the flip-flop and latch are inductors, Zhang teaches such a limitation. Zhang discloses a latch or flip-flop containing inductors as loads. (Fig. 7, labels 722 and 724) It would be obvious to one skilled in the art to use inductors as loads to further improve the bandwidth. (Col. 5, lines 66-67)

b. Regarding **claim 22**, line 1, in Fig. 7, Although Hogge fails to teach a MOSFET circuit, Zhang discloses first and second MOSFETs connected together at the source, their gate terminals coupled to logic signals and drain terminals connected to true and complementary output labeled Vlqn and Vlqp, a first clocked MOSFET connected to the first and second MOSFETs at the drain, a

gate terminal coupled to a clock signal, a third and fourth MOSFETs connected at their source terminals, their gate and drain terminals respectively cross-coupled to the true and complementary output, a second MOSFET having a drain terminal coupled to the source terminals of the third and fourth MOSFETs, a gate terminal connected to a clock signal, a first and second load consisting of resistive and inductive loads and connected to the power supply and true output, a current-source, labeled 450, connected to the first and second clocked MOSFETs and a second power supply. (Fig. 7) It would be obvious to one skilled in this art to provide a synchronized serialized data circuit. (Col. 1, lines 59-61)

c. Regarding **claim 23**, line 1, in Fig. 7, Although Hogge fails to teach a flip-flop as described in claim 23, Zhang discloses a first and second clocked latch wherein the gate terminals are coupled to the true and complementary output of the first clocked latch. (Fig. 7, labels Vlqn and Vlqp) It would obvious to one skilled in this art to provide a circuit that will synchronize data at high frequencies. (Col. 1, lines 59-61)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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